Publications: Dr. Siva Satyendra Sahoo

Important Publications

[ACM TECS '23] S. S. Sahoo, S. Ullah, and A. Kumar. 2023. *AxOTreeS: A Tree Search Approach to Synthesizing FPGA-based Approximate Operators*. **ACM Trans. Embedd. Comput. Syst.** 22, 5s, Article 101 (July 2023), 26 pages. https://doi.org/10.1145/3609096 (Accepted for publication).

[IEEE ESL '23] Y. Zhao, S. Ullah, S. S. Sahoo, & A. Kumar. 2023. *NvMISC: Towards an FPGA-based Emulation Platform for RISC-V and Non-volatile Memories*. **Embedded System Letters** (Accepted for publication).

[ASP-DAC '23] R. Ranjan, S. Ullah, S. S. Sahoo and A. Kumar, *SyFAxO-GeN: Synthesizing FPGA-based Approximate Operators with Generative Networks*, 2023 28th Asia and South Pacific Design Automation Conference (**ASP-DAC '23**), Tokyo, Japan, 2023, pp. 402-409.

[ACM TECS '22] S. Ullah, S. S. Sahoo, N. Ahmed, D. Chaudhury, & A. Kumar. *AppAxO: Designing Application-specific Approximate Operators for FPGA-based Embedded Systems*, in **ACM Trans. Embed. Comput. Syst.** 21, 3, Article 29 (May 2022), 31 pages. https://doi.org/10.1145/3513262.

[DAC '21] S. Ullah, S. S. Sahoo and A. Kumar, *CLAppED: A Design Framework for Implementing Cross-Layer Approximation in FPGA-based Embedded Systems*, 2021 58th ACM/IEEE Design Automation Conference (**DAC '21**), San Francisco, CA, USA, 2021, pp. 475-480, doi: 10.1109/DAC18074.2021.9586260.

[GLSVLSI '21] S. S. Sahoo, A. R. Baranwal, S. Ullah & A. Kumar, *MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems*, in Proceedings of the 2021 on Great Lakes Symposium on VLSI (**GLSVLSI 2021**), 339-346.

[DAC '20] Sahoo, S. S., Veeravalli, B., & Kumar, A. (2020). *CL(R)Early: An Early-stage DSE Methodology for Cross-Layer Reliability-aware Heterogeneous Embedded Systems*. In Proceedings of the 57th Annual Design Automation Conference. **DAC '20**. A Virtual Experience.

[DATE '20] Rai, S., Raitza, M., Sahoo, S. S., & Kumar, A. (2020). *DISCERN: Distilling Standard Cells for Emerging Reconfigurable Nanotechnologies*. In 2020 Design, Automation & Test in Europe Conference & Exhibition, **DATE 2020**, Virtual Conference and Exhibition, April 21- May 31, 2020.

[DAC '19] Sahoo, S. S., Veeravalli, B., & Kumar, A. (2019). *A Hybrid Agent-based Design Methodology for Dynamic Cross-layer Reliability in Heterogeneous Embedded Systems*. In Proceedings of the 56th Annual Design Automation Conference. **DAC '19**. Las Vegas, NV, USA.

[ASP-DAC '18] Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018). *Lifetime-aware design methodology for dynamic partially reconfigurable systems*. In 23rd Asia and South Pacific Design Automation Conference, **ASP-DAC 2018**, Jeju, Korea (South), January 22-25, 2018(pp. 393–398).

A: Peer-reviewed scientific articles

Journals

[J9] S. S. Sahoo, S. Ullah, and A. Kumar. 2023. *AxOTreeS: A Tree Search Approach to Synthesizing FPGA-based Approximate Operators.* **ACM Trans. Embedd. Comput. Syst.** 22, 5s, Article 101 (July 2023), 26 pages. https://doi.org/10.1145/3609096 (Accepted for publication).

[J8] Y. Zhao, S. Ullah, S. S. Sahoo, & A. Kumar. 2023. *NvMISC: Towards an FPGA-based Emulation Platform for RISC-V and Non-volatile Memories.* **Embedded System Letters** (Accepted for publication).

[J7] S. Ullah, S. S. Sahoo, N. Ahmed, D. Chaudhury, & A. Kumar. *AppAxO: Designing Application-specific Approximate Operators for FPGA-based Embedded Systems,* in **ACM Trans. Embed. Comput. Syst.** 21, 3, Article 29 (May 2022), 31 pages. https://doi.org/10.1145/3513262.

[J6] B. Ranjbar, A. Hosseinghorban, S. S. Sahoo, A. Ejlali & A. Kumar. *BOT-MICS: Bounding Time Using Analytics in Mixed-Criticality Systems,* in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2021.3127867.

[J5] S. S. Sahoo, Ranjbar, B., & Kumar, A, *Reliability-aware Resource Management in Multi-/Many-core Systems: A Perspective Paper*, in **MDPI Journal of Low Power Electronics and Applications**, 2021.

[J4] Nambi, S., Ullah, S., Lohana, A., S. S. Sahoo, Merchant, F., & Kumar, A, *ExPAN(N)D: Exploring Posits for Efficient Artificial Neural Network Design in FPGA-based Edge Processing.* in **IEEE Access**, vol. 9, pp. 103691-103708, 2021, doi: 10.1109/ACCESS.2021.3098730.

[J3] A. R. Baranwal, S. Ullah, S. S. Sahoo & A. Kumar, ReLAccS: *A Multi-level Approach to Accelerator Design for Reinforcement Learning on FPGA-based Systems,* in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, doi: 10.1109/TCAD.2020.3028350.

[J2] S. Ullah, H. Schmidl, S. S. Sahoo, S. Rehman & A. Kumar, *Area-optimized Accurate and Approximate Softcore Signed Multiplier Architectures*, in **IEEE Transactions on Computers**, doi: 10.1109/TC.2020.2988404.

[J1] Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A, *Multi-objective design space exploration for system partitioning of FPGA-based Dynamic Partially Reconfigurable Systems,* In **Integration, the VLSI Journal, Elsevier**, November 2018.

Conference Proceedings

[C18] S. Ullah, S. S. Sahoo, and A. Kumar. 2023. *CoOAx: Correlation-aware Synthesis of FPGA-based Approximate Operators.* In Proceedings of the Great Lakes Symposium on VLSI 2023 (**GLSVLSI '23**). Association for Computing Machinery, New York, NY, USA, 671–677. https://doi.org/10.1145/3583781.3590222

[C17] R. Ranjan, S. Ullah, S. S. Sahoo and A. Kumar, *SyFAxO-GeN: Synthesizing FPGA-based Approximate Operators with Generative Networks*, 2023 28th Asia and South Pacific Design Automation Conference (**ASP-DAC '23**), Tokyo, Japan, 2023, pp. 402-409.

[C16] A. Immaneni, S. Ullah, S. Nambi, S. S. Sahoo and A. Kumar, *PosAx-O: Exploring Operator-level Approximations for Posit Arithmetic in Embedded AI/ML,*" in 2022 25th Euromicro Conference on Digital System Design (**Euromicro DSD '22**), Maspalomas, Spain, 2022 pp. 214-223. doi: 10.1109/DSD57027.2022.00037

[C15] S. S. Sahoo, A. Kumar, M. Decky, S. C. B. Wong, G. V. Merrett, Y. Zhao, Jiachen Wang, X. Wang & A. K. Singh, *Emergent design challenges for embedded systems and paths forward: mixed-criticality, energy, reliability and security perspectives*, in Proceedings of the 2021 International Conference on Hardware/Software Codesign and System Synthesis (**CODESS, ESWeek 2021**). Association for Computing Machinery, New York, NY, USA, 1–10. DOI:https://doi.org/10.1145/3478684.3479246

[C14] S. S. Sahoo & A. Kumar, *Using Monte Carlo Tree Search for EDA – A Case-study with Designing Cross-layer Reliability for Heterogeneous Embedded Systems*, in 2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (**VLSI-SoC 2021**), 2021, pp. 1-6, doi: 10.1109/VLSI-SoC53125.2021.9606987.

[C13] S. S. Sahoo & A. Kumar, *CLEO-CoDe: Exploiting Constrained Decoding for Cross-Layer Energy Optimization in Heterogeneous Embedded Systems*, in 2021 IFIP/IEEE 29th International Conference on Very Large Scale Integration (**VLSI-SoC 2021**), 2021, pp. 1-6, doi: 10.1109/VLSI-SoC53125.2021.9606983.

[C12] S. S. Sahoo, A. R. Baranwal, S. Ullah & A. Kumar, *MemOReL: A Memory-oriented Optimization Approach to Reinforcement Learning on FPGA-based Embedded Systems*, in Proceedings of the 2021 on Great Lakes Symposium on VLSI (**GLSVLSI 2021**), 339-346.

[C11] S. Ullah, S. S. Sahoo and A. Kumar, *CLAppED: A Design Framework for Implementing Cross-Layer Approximation in FPGA-based Embedded Systems*, 2021 58th ACM/IEEE Design Automation Conference (**DAC '21**), San Francisco, CA, USA, 2021, pp. 475-480, doi: 10.1109/DAC18074.2021.9586260.

[C10] Ranjbar, B., Hoseinghorban, A., Sahoo, S. S., Ejlali, A. & Kumar, A. (2020). *Improving the Timing Behaviour of Mixed-Criticality Systems Using Chebyshev's Theorem*. In Design, Automation & Test in Europe Conference & Exhibition, **DATE 2021**, Virtual Conference and Exhibition, February 01-05, 2021.

[C9] S. S. Sahoo, B. Veeravalli and A. Kumar, *Markov Chain-based Modeling and Analysis of Checkpointing with Rollback Recovery for Efficient DSE in Soft Real-time Systems*. (2020) IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT 2020**), Frascati, Italy, 2020, pp. 1-6, doi: 10.1109/DFT50435.2020.9250892.

[C8] Sahoo, S. S., Veeravalli, B., & Kumar, A. (2020). *CL(R)Early: An Early-stage DSE Methodology for Cross-Layer Reliability-aware Heterogeneous Embedded Systems*. In Proceedings of the 57th Annual Design Automation Conference. **DAC '20**. A Virtual Experience.

[C7] Rai, S., Raitza, M., Sahoo, S. S., & Kumar, A. (2020). *DISCERN: Distilling Standard Cells for Emerging Reconfigurable Nanotechnologies*. In 2020 Design, Automation & Test in Europe Conference & Exhibition, **DATE 2020**, Virtual Conference and Exhibition, April 21- May 31, 2020.

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[C5] Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018). *QoS-aware Cross-layer Reliability-integrated FPGA-based Dynamic Partially Reconfigurable System Partitioning*. In International Conference on Field-Programmable Technology, **ICFPT 2018**, Naha, Okinawa, Japan, December 10-14, 2018.

[C4] Sahoo, S. S., Nguyen, T. D. A., Veeravalli, B., & Kumar, A. (2018). *Lifetime-aware design methodology for dynamic partially reconfigurable systems*. In 23rd Asia and South Pacific Design Automation Conference, **ASP-DAC 2018**, Jeju, Korea (South), January 22-25, 2018(pp. 393–398).

[C3] Sahoo, S. S., Veeravalli, B., & Kumar, A. (2018). *CLRFrame: An analysis framework for designing cross-layer reliability in embedded systems*. In 31st International Conference on VLSI Design and 17th International Conference on Embedded Systems, **VLSID 2018**, Pune, India, January 6-10, 2018 (pp. 307–312).

[C2] Sahoo, S. S., Kumar, A., & Veeravalli, B. (2016). *Design and evaluation of reliability-oriented task remapping in MPSoCs using time-series analysis of intermittent faults.* In 2016 Design, Automation & Test in Europe Conference & Exhibition, **DATE 2016**, Dresden, Germany, March 14-18, 2016 (pp. 798–803).

[C1] Sahoo, S. S., Veeravalli, B., & Kumar, A. (2016). *Cross-layer fault-tolerant design of real-time systems.* In 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, **DFT 2016**, Storrs, CT, USA, September 19-20, 2016 (pp. 63–68).

B: Non-refereed scientific articles

Book Chapters

[Ch3] S. Ullah, S. S. Sahoo, & A. Kumar, *Efficient Hardware Arithmetic for Embedded Machine Learning*, in **Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing, Springer 2023**. *To appear.*

[Ch2] Ranjbar, B., Sahoo, S. S., Singh, A., Dziurzanski, P., & Kumar, A., *Power management of Multicore systems*, in **Handbook of Computer Architecture, Springer 2023**. *To appear.*

[Ch1] Sahoo, S. S., Das, A. & Kumar, A., *Fault-tolerant Computer Architectures*, in **Handbook of Computer Architecture, Springer 2023**. *To appear.*

G: Theses & Degree Projects

[Doctoral Dissertation] Sahoo, Siva Satyendra. *A Cross-Layer Reliability-Integrated System-Level Design Methodology for Heterogeneous Multiprocessor SoC-Based Embedded Systems.* Diss. National University of Singapore (Singapore), 2019.

[M.Tech Project] Sahoo, Siva Satyendra and Arun Ajith S.. *Hardware Accelerator for Support Vector Machine.* Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore (India), 2012.

[B.Tech Project] Sahoo, Siva Satyendra, Sruti Ranjan Sahoo and Pranab Shankar Nayak. *Short Message Service (SMS)-based Home Automation.* Department of Instrumentation and Electronics, College of Engineering and Technology, Bhubaneswar (India), 2008.